- **Zero Reading for 0-V Input**
- **Precision Null Detection With True Polarity at Zero**
- **1-pA Typical Input Current**
- **True Differential Input**
- **Multiplexed Binary-Coded-Decimal (BCD) Output**
- **Low Rollover Error: ±1 Count Max**
- **Control Signals Allow Interfacing With UARTs or Microprocessors**
- **Autoranging Capability With Over-and Under-Range Signals**
- **TTL-Compatible Outputs**
- **Second Source to Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix Si7135**
- **CMOS Technology**

DW OR N PACKAGE
(TOP VIEW)

V_{CC-}	1	28	UNDER RANGE
REF	2	27	OVER RANGE
ANLG COMMON	3	26	$\overline{STROBE}$
INT OUT	4	25	RUN/$\overline{HOLD}$
AUTO ZERO	5	24	DGTL GND
BUFF OUT	6	23	POLARITY
C_{ref-}	7	22	CLK
C_{ref+}	8	21	BUSY
IN−	9	20	D1
IN+	10	19	D2
V_{CC+}	11	18	D3
D5	12	17	D4
B1	13	16	B8
B2	14	15	B4
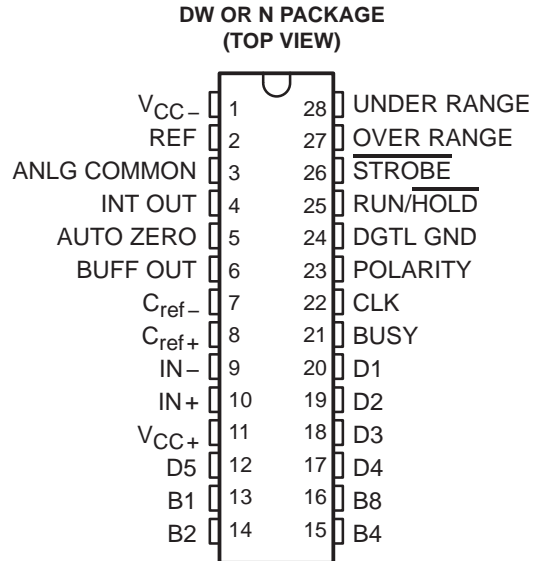
DESCRIPTION

The ICL7135C and TLC7135C converters are manufactured with Texas Instruments highly efficient CMOS technology. These 4 1/2-digit, dual-slope-integrating, analog-to-digital converters (ADCs) are designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs B1, B2, B4, and B8 provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135C and TLC7135C offer 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 μV and zero drift is less than 0.5 μV/°C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ±1 count.

The BUSY, $\overline{STROBE}$, RUN/$\overline{HOLD}$, OVER RANGE, and UNDER RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer through universal asynchronous receiver transmitters (UARTs).

The ICL7135C and TLC7135C are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

	PACKAGE		
T_A	PLASTIC DIP (N)	SMALL OUTLINE (DW)	
0°C to 70°C	ICL7135CN		
	TLC7135CN	TLC7135CDW	

Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handliling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

FUNCTIONAL BLOCK DIAGRAM

DIGITAL SECTION

ANALOG SECTION
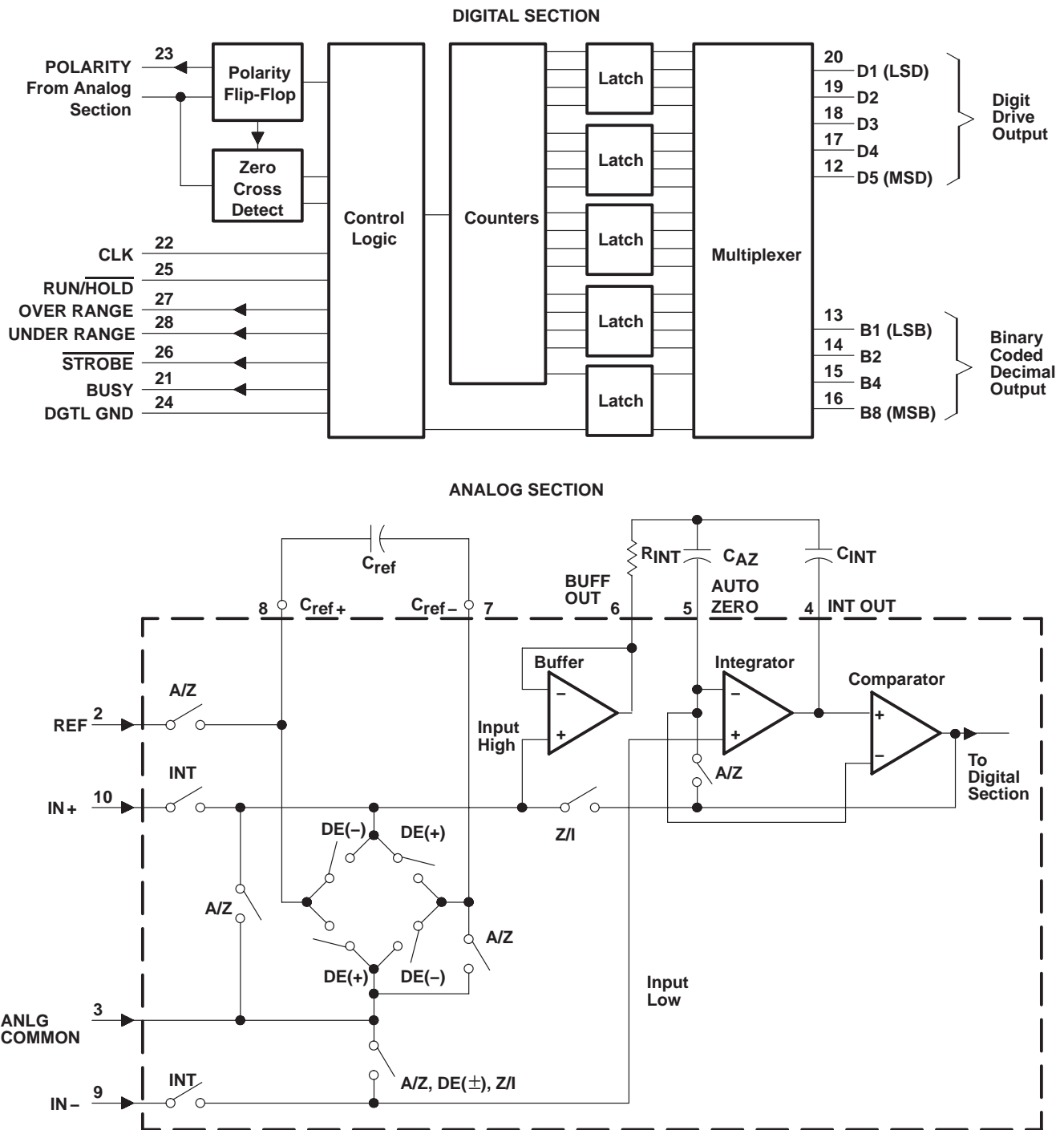
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

	UNIT
Supply voltage (V_{CC+} with respect to V_{CC-})	15 V
Analog input voltage (IN– or IN+)	V_{CC-} to V_{CC+}
Reference voltage range	V_{CC-} to V_{CC+}
Clock input voltage range	0 V to V_{CC+}
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package	260°C

[1] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	−3	−5	−8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IH}	2.8			V
Low-level input voltage, CLK, RUN/$\overline{HOLD}$, V_{IL}			0.8	V
Differential input voltage, V_{ID}	V_{CC-} +1		V_{CC+} −0.5	V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0		70	°C

NOTE 1: Clock frequency range extends down to 0 Hz.

ELECTRICAL CHARACTERISTICS

V_{CC+} = 5 V, V_{CC-} = 5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D1-D5, B1,B2,B4,B8	I_O = −1 mA	2.4		5	V
		Other outputs	I_O = −10 μA	4.9		5	
V_{OL}	Low-level output voltage		I_O = 1.6 mA			0.4	V
$V_{ON(PP)}$	Peak-to-peak output noise voltage (see Note 1)		V_{ID} = 0, Full scale = 2 V		15		μV
α_{VO}	Zero-reading temperature coefficient of output voltage		V_{ID} = 0, 0°C ≤ T_A ≤ 70°C		0.5	2	μV/°C
I_{IH}	High-level input current		V_I = 5 V, 0°C ≤ T_A ≤ 70°C		0.1	10	μA
I_{IL}	Low-level input current		V_I = 0 V, 0°C ≤ T_A ≤ 70°C		−0.02	−0.1	mA
I_I	Input leakage current, IN– and IN+		V_{ID} = 0	T_A = 25°C		1	10	pA
				0°C ≤ T_A ≤ 70°C			250	
I_{CC+}	Positive supply current		f_{clock} = 0	T_A = 25°C		1	2	mA
				0°C ≤ T_A ≤ 70°C			3	
I_{CC-}	Negative supply current		f_{clock} = 0	T_A = 25°C		−0.8	−2	mA
				0°C ≤ T_A ≤ 70°C			−3	
C_{pd}	Power dissipation capacitance		See Note 2		40		pF

NOTES: 1. This is the peak-to-peak value that is not exceeded 95% of the time.
      2. Factor-relating clock frequency to increase in supply current. At V_{CC+} = 5 V, I_{CC+} = I_{CC+}(f_{clock} = 0) + $C_{pd} \times 5$ V $\times f_{clock}$

TEXAS
INSTRUMENTS
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OPERATING CHARACTERISTICS

V_{CC+} = 5 V, V_{CC-} = 5 V, V_{ref} = 1 V, f_{clock} = 120 kHz, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
α_{FS}	Full-scale temperature coefficient (see Note 1)	V_{ID} = 2 V, $\quad$ 0°C ≤ T_A ≤ 70°C			5	ppm/°C
E_L	Linearity error	−2 V ≤ V_{ID} ≤ 2 V		0.5		count
E_D	Differential linearity error (see Note 2)	−2 V ≤ V_{ID} ≤ 2 V		0.01		LSB
E_{FS}	± Full-scale symmetry error (rollover error) (see Note 3)	V_{ID} = ±2 V		0.5	1	count
	Display reading with 0-V input	V_{ID} = 0, $\quad$ 0°C ≤ T_A ≤ 70°C	−0.0000	±0.0000	0.0000	Digital Reading
	Display reading in ratiometric operation	V_{ID} = V_{ref}, $\quad$ T_A = 25°C	0.9998	0.9999	1.0000	Digital Reading
		0°C ≤ T_A ≤ 70°C	0.9995	0.9999	1.0005	

NOTES: 1. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/°C.
2. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.
3. Rollover error is the difference between the absolute values of the conversion for 2 V and −2 V.

TIMING DIAGRAMS
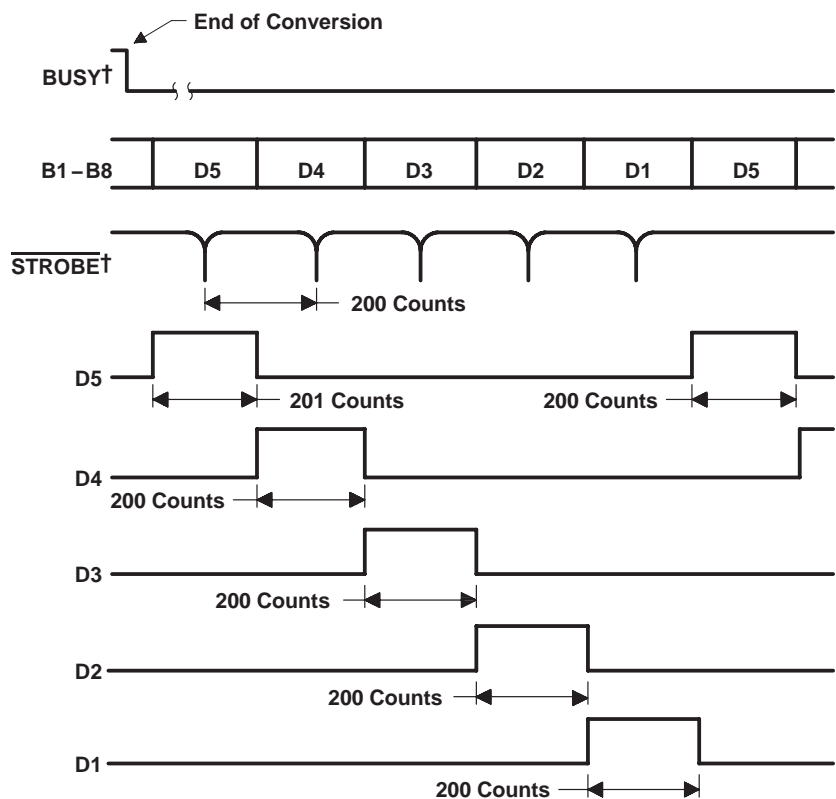
† Delay between BUSY going low and the first STROBE pulse is dependent upon the analog input.
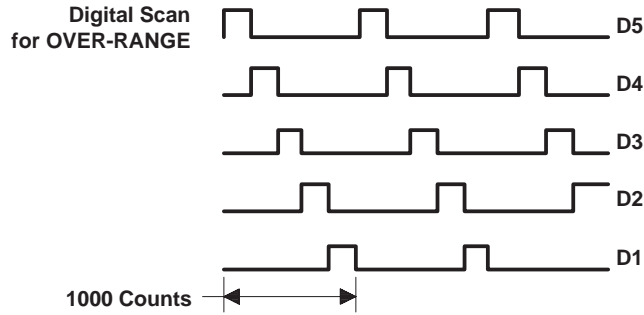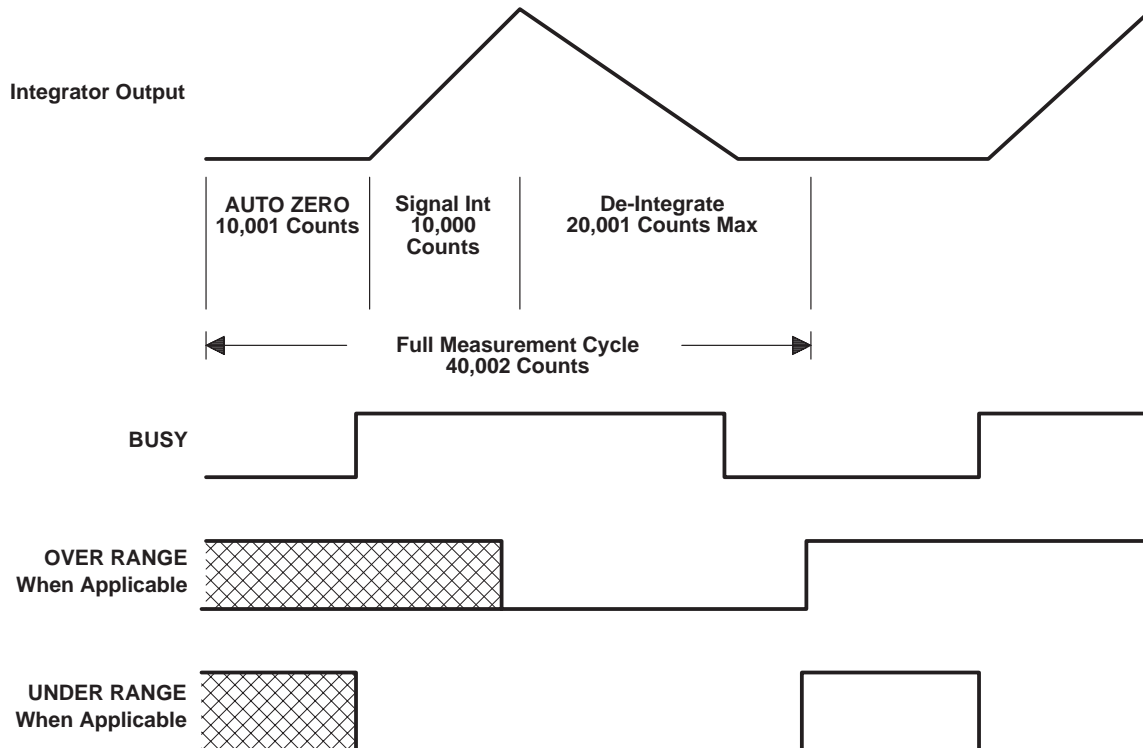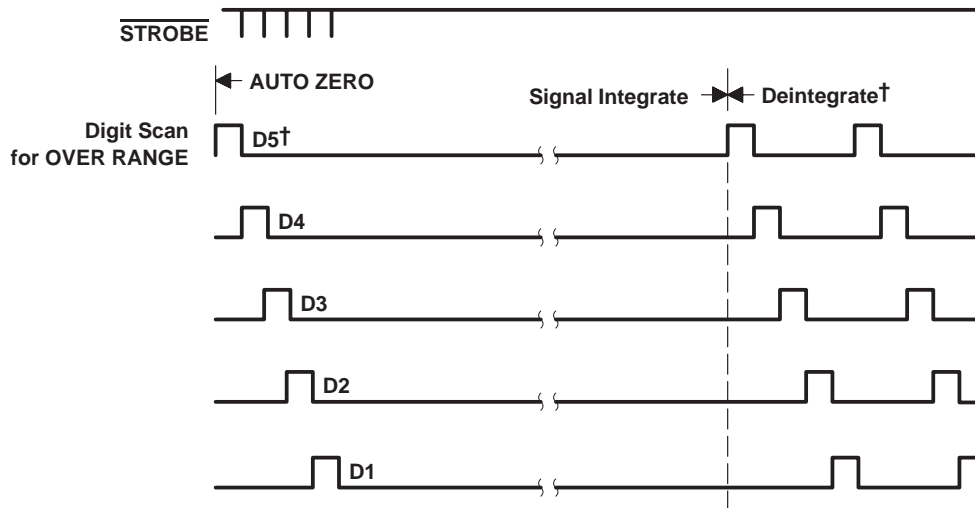
Figure 1

Figure 2

Figure 3

† First D5 of AUTO ZERO and deintegrate is one count longer.

Figure 4

PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135C and TLC7135C consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN− inputs are disconnected from the terminals and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μV.

2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN− inputs are connected to the external terminals. The differential voltage between these inputs is integrated for a fixed period of time. When the input signal has no return with respect to the converter power supply, IN− can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.

3. Deintegrate Phase. The reference is used to perform the deintegrate task. The internal IN− is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal ensures that the capacitor is connected with the correct polarity so that the integrator output polarity returns to zero. The time required for the output to return to zero is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation $10{,}000 \times (V_{ID}/V_{ref})$. The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref}.

4. Zero Integrator Phase. The internal IN− is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically, this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

![Texas Instruments logo]
TEXAS INSTRUMENTS

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DESCRIPTION OF ANALOG CIRCUITS

Input Signal Range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common-mode rejection ratio (CMRR) is typically 86 dB. Both differential and common-mode voltages cause the integrator output to swing. Therefore, care must be exercised to ensure that the integrator output does not become saturated.

Analog Common

Analog common (ANLG COMMON) is connected to the internal IN– during the auto-zero, deintegrate, and zero integrator phases. When IN– is connected to a voltage that is different from analog common during the signal integrate phase, the resulting common-mode voltage is rejected by the amplifier. However, in most applications, IN– is set at a known fixed voltage (i.e., power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. Removing the common-mode voltage in this manner slightly increases conversion accuracy.

Reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

DESCRIPTION OF DIGITAL CIRCUITS

RUN/$\overline{\text{HOLD}}$ Input

When RUN/$\overline{\text{HOLD}}$ is high or open, the device continuously performs measurement cycles every 40,002 clock pulses. When this input is taken low, the integrated circuit continues to perform the ongoing measurement cycle and then hold the conversion reading for as long as the terminal is held low. When the terminal is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) initiates a new measurement cycle. When this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first $\overline{\text{STROBE}}$ pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurement after the first $\overline{\text{STROBE}}$ pulse.

$\overline{\text{STROBE}}$ Input

Negative going pulses from this input transfer the BCD conversion data to external latches, UARTs, or microprocessors. At the end of the measurement cycle, $\overline{\text{STROBE}}$ goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD terminals. After the first 101 counts, halfway through the duration of output D1–D5 going high, the $\overline{\text{STROBE}}$ terminal goes low for 1/2 clock pulse width. The placement of the $\overline{\text{STROBE}}$ pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the $\overline{\text{STROBE}}$ pulse also ensures that the BCD bits for the second MSD are not yet competing for the BCD lines and latching of the correct bits is ensured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines continue scanning without the inclusion of $\overline{\text{STROBE}}$ pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

BUSY Output

The BUSY output goes high at the beginning of the signal integrate phase. BUSY remains high until the first clock pulse after zero crossing or at the end of the measurement cycle when an over-range condition occurs. It is possible to use the BUSY terminal to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses that occur during the deintegrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE Output

When an over-range condition occurs, this terminal goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER RANGE output goes high at the end of BUSY and goes low at the beginning of the deintegrate phase in the next measurement cycle.

UNDER-RANGE Output

At the end of the BUSY signal, this terminal goes high when the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER-RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

POLARITY Output

The POLARITY output is high for a positive input signal and updates at the beginning of each deintegrate phase. The polarity output is valid for all inputs including ±0 and OVER RANGE signals.

Digit-Drive (D1, D2, D4 and D5) Outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit-drive outputs are blanked from the end of the strobe sequence until the beginning of the deintegrate phase (when the sequential digit-drive activation begins again). The blanking activity during an over-range condition can cause the display to flash and indicate the over-range condition.

BCD Outputs

The BCD bits (B1, B2, B4 and B8) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate digit-drive line for the given digit is activated.

System Aspects

Integrating Resistor

The value of the integrating resistor (R_{INT}) is determined by the full-scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 μA of current with negligible nonlinearity. The equation for determining the value of this resistor is:

$$R_{INT} = \frac{\text{Full Scale Voltage}}{I_{INT}}$$

Integrating amplifier current, I_{INT}, from 5 to 40 μA yields good results. However, the nominal and recommended current is 20 μA.

**TEXAS
INSTRUMENTS**

Integrating Capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. When the amplifier output is within 0.3 V of either supply, saturation occurs. With ±5-V supplies and ANLG COMMON connected to ground, the designer should design for a ±3.5-V to ±4-V integrating amplifier swing. A nominal capacitor value is 0.47 µF. The equation for determining the value of the integrating capacitor (C_{INT}) is:

$$C_{INT} = \frac{10,000 \times \text{Clock Period} \times I_{INT}}{\text{Integrator Output Voltage Swing}}$$

where

I_{INT} is nominally 20 µA.

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor that is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and deintegrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and polycarbonate capacitors have higher dielectric absorption, but also work well.

Auto-Zero and Reference Capacitor

Large capacitors tend to reduce noise in the system. Dielectric absorption is unimportant except during power up or overload recovery. Typical values are 1 µF.

Reference Voltage

For high-accuracy absolute measurements, a high quality reference should be used.

Rollover Resistor and Diode

The ICL7135C and TLC7135C have a small rollover error; however, it can be corrected. The correction is to connect the cathode of any silicon diode to INT OUT and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions, the resistor value is 100 kΩ. This value may be changed to correct any rollover error that has not been corrected. In many noncritical applications the resistor and diode are not needed.

Maximum Clock Frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3-µs delay. Therefore, with a 160-kHz clock frequency (6-µs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading changes from 0 to 1 with a 50-µV input, 1 to 2 with a 150-µV input, 2 to 3 with a 250-µV input, etc. This transition at midpoint is desirable; however, when the clock frequency is increased appreciably above 160 kHz, the instrument flashes 1 on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

When the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since nonlinearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay are a constant and can be subtracted out digitally.

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the deintegrate phase, and thus compensates for the comparator delay. This series resistor should be 10 Ω to 50 Ω. This approach allows clock frequencies up to 480 kHz.

Minimum Clock Frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 µs are not influenced by leakage error.

Rejection of 50-Hz or 60-Hz Pickup

To maximize the rejection of 50-Hz or 60-Hz pickup, the clock frequency should be chosen so that an integral multiple of 50-Hz or 60-Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies that can be used are:

50 Hz: 250, 166.66, 125, 100 kHz, etc.

60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

Zero-Crossing Flip-Flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle has occurred, so any comparator transients that result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the deintegrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

Noise

The peak-to-peak noise around zero is approximately 15 µV (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 µV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

Analog and Digital Grounds

For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

Power Supplies

The ICL7135C and TLC7135C are designed to work with ±5-V power supplies. However, 5-V operation is possible when the input signal does not vary more than ±1.5 V from midsupply.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ICL7135CN	ACTIVE	PDIP	N	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
ICL7135CNG4	ACTIVE	PDIP	N	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
TLC7135CDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7135CDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7135CDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7135CDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC7135CN	ACTIVE	PDIP	N	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
TLC7135CNG4	ACTIVE	PDIP	N	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 Q2
Q3 Q4

Q1 Q2
Q3 Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7135CDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7135CDWR	SOIC	DW	28	1000	346.0	346.0	49.0

DW (R−PDSO−G28)   PLASTIC SMALL−OUTLINE PACKAGE
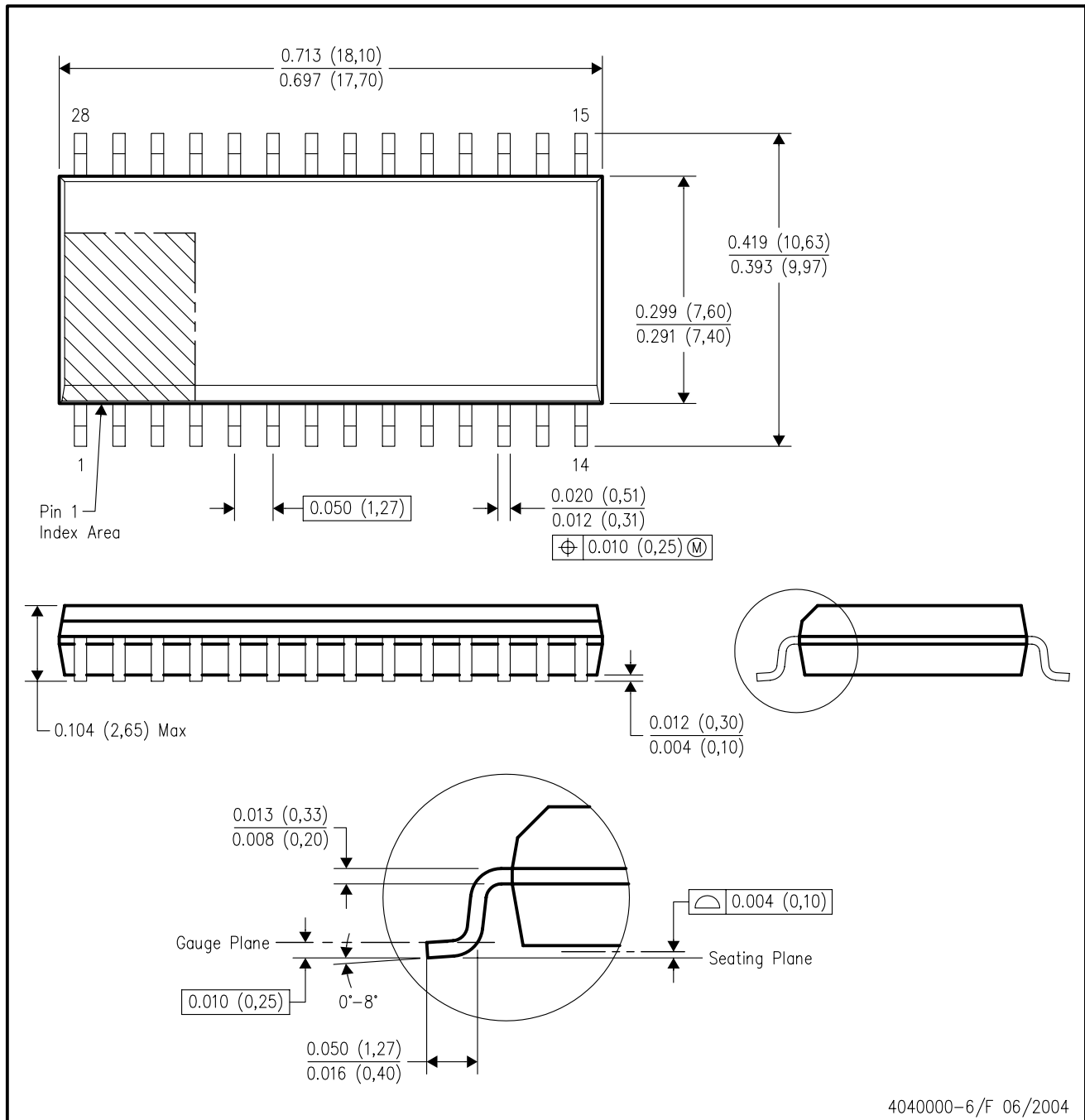
0.713 (18,10)
0.697 (17,70)

28   15

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1   14

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040000−6/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AE.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

PINS ** DIM	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)